U.S. Serial No.: 09/911,780

Group Art Unit: 2674

Examiner: Jean E Lesperance Pg.9

**REMARKS** 

Claims 1-8 are in the present application pending.

I. FORMAL MATTERS

Applicant notes with appreciation that the Final Office Action again acknowledges the claim to foreign priority under 35 U.S.C. § 119(a)-(d) or (f) and indicates that the certified copies of the priority documents have been received.

The Office Action does <u>not</u> indicate whether the drawings filed on July 31, 2001 are acceptable. <u>Applicant respectfully requests the examiner to do so.</u>

The Office Action includes a copy of the PTO Form 1449 that was submitted with the Information Disclosure Statement filed on December 19, 2003. Each reference is initialed, thereby indicating that each reference was considered by the Examiner. The present Office Action, and the First Office Action dated March 17, 2003, do <u>not</u> include a copy of the PTO Form 1449 that was submitted with the Information Disclosure Statement filed on July 24, 2001. <u>Applicant respectfully requests the Examiner to send to the undersigned a copy of this PTO Form 1449 with each reference initialed by the Examiner.</u>

II. PRIOR ART REJECTION

The Examiner has rejected claims 1-8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,025,822 (Motegi). This rejection is traversed.

U.S. Serial No.: 09/911,780

Group Art Unit: 2674

Examiner: Jean E Lesperance

- 8. - -

driving circuits are connected in series, i.e. the input of a second column electrode

The characterizing feature of claims 1-5 is that the plurality of column electrode

driving circuit is connected to the output of a first column electrode driving circuit,

and so on, and hence the timing signals are passed between the column electrode

driving circuits in a cascade manner.

This arrangement has the advantages of decreasing the size of the display device

and allowing the devices to be produced more easily.

The Examiner asserts that Fig. 7 of Motegi shows a controller (23) connected to

the column drivers (21) connected in series with each other and row electrode drivers

(22) connected in series with each other. Applicant submits that the controller 23 is not

a common electrode driving circuit. Also, Applicant submits that the column drivers 21

are connected in **parallel**, and **not** in series, as shown in Fig. 7 of Motegi, which is

opposite to the configuration of the present invention, as shown in Fig. 2 of the present

application.

Further, with respect to the claim elements of data input section, data output

section and selection section, the Examiner has not identified any particular

components in Motegi, et al. that correspond to each of these element or the

relationship therebetween.

Motegi, et al. certainly does not disclose a selection section for selecting one of a

signal in synchronization with the timing signal and the control data signal input to

the data input section, or a data output section for outputting the selected signal to

the data input section of a second column electrode driving circuit.

U.S. Serial No.: 09/911,780

Group Art Unit: 2674

Examiner: Jean E Lesperance Pg.11

Regarding claim 6, the Examiner asserts that the controller 2 in Fig. 6 outputs

the claimed timing signal. Applicant submits that Fig. 6 illustrates the controller 2 as

a simple block and does not show a timing signal that is supplied on the specific path

defined in claim 6. Therefore, Applicant submits that the Examiner has failed to

identify any portion of Motegi that teaches this feature of claim 6. Also, in the

rejection of claim 6, the examiner relies on Fig. 7 and Fig. 1. Fig. 1 shows an

embodiment of the invention. Fig. 7 shows a prior art LCD. Applicant submits that

the Examiner has failed to assert reasons why it would have been obvious to combine

features of the prior art LCD with the invention. Therefore, Applicant submits that the

Examiner has not formed a prima facie case of obviousness.

Regarding claim 7, the Examiner asserts that the controller 23 in Fig. 7 outputs

the claimed timing signal. Applicant submits that Fig. 7 illustrates the controller 23

as a simple block and does not show a timing signal that is supplied on the specific

path defined in claim 7. Therefore, Applicant submits that the Examiner again has

failed to identify any portion of Motegi that teaches this feature of claim 7. Therefore,

Applicant submits that the Examiner has not formed a prima facie case of

obviousness.

Regarding claim 8, Applicant submits that Motegi does not teach or suggest a

timing signal that is output from a first column electrode driving circuit and supplied

to a first row electrode driving circuit sequentially through a circuit board so as not to

U.S. Serial No.: 09/911,780

Group Art Unit: 2674

Examiner: Jean E Lesperance Pg. 12

be crossed with a signal circuit, as recited by claim 8. In fact, the examiner admits that the first column electrode driving circuit does not generate a timing signal.

Therefore, Applicant submits that the Examiner has not formed a prima facie case of obviousness with respect to claim 8.

Also regarding claim 8, the Examiner asserts that Fig. 7 of Motegi includes column drivers 21 connected in series and row electrode drivers 22 connected in series. However, Applicant submits that, as shown in Fig. 7 of Motegi, the column drivers 21 and row drivers 22 are connected in **parallel**. Therefore, Applicant submits that the Examiner's assertions regarding the Motegi reference are incorrect. Accordingly, the rejections under 35 U.S.C. § 103(a) are improper and should be withdrawn.

Likewise, with respect to claims 6 – 8, the Examiner has asserted that the configuration is disclosed in Motegi et al., but the Examiner has failed to identify any specific support in Motegi, et al. for his contention, in the figures or description.

Further, since claims 6 – 8 are amended to include the feature of "connected in series", they are distinguished over Motegi, et al. for at least the above reason.

Based on the foregoing, Applicant submits that the present application is now in condition for allowance, and allowance is respectfully solicited. Examiner is invited to call the undersigned at the telephone number listed below to discuss any of the

U.S. Serial No.: 09/911,780

Group Art Unit: 2674

Examiner: Jean E Lesperance Pg. 13

outstanding issues of the present application if the Examiner believes that such

discussion would expedite the allowance of the present application.

Applicant believes that no additional fees are due for the subject application.

However, if for any reason a fee is required, a fee paid is inadequate or credit is owed

for any excess fee paid, you are hereby authorized and requested to charge Deposit

Account No. **04-1105**.

Respectfully submitted,

Date: April 28, 2004

Customer No.: 21874

John J. Penny, or. Reg. No. 36,984

Intellectual Property Practice Group of

EDWARDS & ANGELL, LLP

P. O. Box 55874 Boston, MA 02205

BOS2\_441185